REMARKS

In the Office Action the Examiner objected to the disclosure for not having a summary, objected to claims 3-5 and 8-14 for informalities, and rejected all claims 1-14 under 35 U.S.C. 102 for being anticipated. Claims 1-14 remain in the application.

With regard to the summary not being present, the Examiner quoted from the MPEP which states that the summary "should precede ..." This is clearly permissive language no the language of a requirement. This language makes it clear that the summary is not required. Further, the Examiner's position is contrary to USPTO practice. US patents are routinely issuing without summaries.

With regard to the informalities in the claims, the Examiner's comments were specifically with respect to claims 3, 8, 10, and 12. All of these claims have been amended in the manner suggested by the Examiner.

With regard to the rejection for anticipation, the Examiner cited Ngu. All of the independent claims have been amended to distinguish from Ngu. Ngu describes only a "last-address" pointer. In this regard, it is not clear which address the pointer is for. Is it for the address of the last data received, the last prefetch address, or something else? In any event there is only one pointer. All of the claims now claim at least two pointers. Some claim three. There is nothing in Ngu to suggest that there should be more than one. Accordingly, Applicants submit that the claims as amended are patentably distinct from Ngu.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning this application.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Motorola, Inc.
Law Department

Customer Number: 23125

By: James L. Clingan, Jr.

James L. Clingan, Jr.
Attorney of Record
Reg. No.: 30,163
Telephone: (512) 996-6839
Fax No.: (512) 996-6854
Email: Jim.Clingan@Motorola.com

CLAIMS - VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for filling a line in a cache, comprising the steps of:

sending a request for data to be provided on a data bus to the cache at a first address;

sending a first request external to the cache for first data at the first address;

defining a first pointer for the first address;

sending for additional data at additional addresses, the additional addresses being consecutive with the first address;

defining a second pointer for the address of the data that was last sent for;

receiving the first data located at the first address;

placing the first data in the line in the cache and onto the data bus;

loading the additional data into the line in the cache as it is received;

defining a third pointer for the address of the data that was last received;

terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses; and

sending the second request external to the cache for the different data at the different address.

3. (Amended) A method for operating a processing system comprising a cache and a processor, comprising the steps of:

generating a first request for data from the cache at a fetch address;

providing the fetch address for a memory that is outside of the cache if there is a miss in the cache;

setting a first pointer for the fetch address;

continuously providing prefetch addresses consecutive with the fetch address for the memory;

setting a second pointer for the latest prefetch address;

generating a second request for data that is different from the prefetch addresses that have been provided; and

terminating the providing of prefetch addresses in response to the second request.

6. (Amended) A processing system, comprising:

a processor for generating data requests at address locations from an external memory that is external to the processing system;

a cache, coupled to the processor, for storing data corresponding to at least some of the address locations;

fetch means, coupled to the cache and the processor, for providing a fetch address for the external memory in response to a request from the processor that results in a miss in the cache, providing requests for the external memory for data at additional addresses that are consecutive with the fetch address in response to receiving the request for the fetch address, tracking progress of the requests for the data at the additional addresses by setting a first pointer for the fetch address and a second pointer for the last address of the additional addresses that was sent out, and terminating the requests for the data at the additional addresses in response to receiving a data request from the processor for data at an address that is different from any of the additional addresses.

8. (Amended) The processing system of claim 7, wherein the cache is characterized as having a plurality of lines that each comprise locations having consecutive addresses, and wherein the additional addresses requested by the fetch means are for locations in the cache that are in a line in the plurality of lines.

10. (Amended) A processing system comprising:[:]

a cache for storing data and providing a hit signal if a request for data is contained in the cache and a miss signal if the request for data is not contained in the cache;

processor means, coupled to the [cached] cache, for sending a request for data to the cache at a first address;

fetch means, coupled to the cache and the processor means, for sending the request external to the cache for first data at a first address in response to the miss signal, sending for additional data at additional addresses, the additional addresses being consecutive with the first address, receiving the first data located at the first address, placing the first data in the cache and onto the data bus, loading the additional data into the line as it is received, tracking progress of the requests for

the data at the additional addresses by setting a first pointer for the first address, a second pointer for the address of the additional addresses that was last sent out, and a third pointer for the address of the additional addresses of the additional data that was last loaded, and terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses.

12. (Amended) The processing system of claim 11, wherein the [cached] cache is characterized as having plurality of lines that each comprise locations having consecutive addresses, and wherein the additional addresses requested by the fetch means are for locations in the cache that are in a line in the plurality of lines.